1. A method to form an integrated circuit device comprising:

forming a dielectric layer overlying a semiconductor substrate;

forming an intrinsic semiconductor layer overlying said dielectric layer;

patterning said intrinsic semiconductor layer;

forming a p+ region in said intrinsic semiconductor layer;

forming an n+ region in said intrinsic semiconductor layer wherein said p+ region and said n+ region are laterally separated by an intrinsic region to thereby form a PIN diode device; and

forming a source region and a drain region in said semiconductor substrate to thereby complete a MOSFET device wherein said PIN diode device is a gate electrode for said MOSFET device.

2. The method according to Claim 1 wherein said dielectric layer comprises an oxide.

3. The method according to Claim 1 wherein said semiconductor layer comprises polysilicon.

4. The method according to Claim 1 wherein said semiconductor layer comprises amorphous silicon.

5. The method according to Claim 1 wherein step of forming said p+ region comprises implanting ions and wherein a masking layer is used to control where said ions are implanted.

6. The method according to Claim 1 wherein said step of forming said n+ region comprises implanting ions and wherein a masking layer is used to control where said ions are implanted.

7. The method according to Claim 6 wherein said step of forming said source and drain regions comprises implanting ions and wherein said step is simultaneous with said step of forming said n+ region.

8. The method according to Claim 1 further comprising:

forming spacers on the sidewalls of said PIN diode device;

forming a masking layer covering said intrinsic region while exposing said p+ region, said n+ region, said source region, and said drain region;

depositing a metal layer overlying said source region, drain region, said n+ region, said p+ regions, said spacers, and said masking layer;

annealing said metal layer to form metal silicide regions overlying said source region, said drain region, said n+ region, and said p+ region; and

removing unreacted said metal layer.

9. The method according to Claim 1 wherein said drain region and said p+ region are connected together to form a first terminal and wherein said source region and said n+ region are connected together to form a second terminal.

10. The method according to Claim 9 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.

11. The method according to Claim 1 wherein said p+ region is a first terminal, wherein said drain region and said n+ region are connected together, and wherein said source region forms a second terminal.

12. The method according to Claim 11 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.

13. An integrated circuit device comprising:

a dielectric layer overlying a semiconductor substrate;

a PIN diode device overlying said dielectric layer wherein said PIN diode device comprises a semiconductor layer having a p+ region and an n+ region that are laterally separated by an intrinsic region; and

a MOSFET device comprising a source region and a drain region in said semiconductor substrate wherein said PIN diode device is a gate electrode for said MOSFET device.

14. The device according to Claim 13 wherein said dielectric layer comprises an oxide.

15. The device according to Claim 13 wherein said semiconductor layer comprises polysilicon.

16. The device according to Claim 13 further comprising:

spacers on the sidewalls of said PIN diode device; and metal silicide regions overlying said source region, said drain region, said n+ region, and said p+ region.

17. The device according to Claim 13 wherein said drain region and said p+ region are connected together to form a first terminal and wherein said source region and said n+ region are connected together to form a second terminal.

18. The device according to Claim 17 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.

19. The device according to Claim 13 wherein said p+ region is a first terminal, wherein said drain region and said n+ region are connected together, and wherein said source region forms a second terminal.

20. The device according to Claim 19 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.

21. An ESD protection device comprising:

a dielectric layer overlying a semiconductor substrate;

a PIN diode device overlying said dielectric layer wherein said PIN diode device comprises a semiconductor layer having a p+ region and an n+ region that are laterally separated by an intrinsic region; and

a MOSFET device comprising a source region and a drain region in said semiconductor substrate, wherein said PIN diode device is a gate electrode for said MOSFET device, wherein said drain region and said p+ region are connected together to form a first terminal, and wherein said source region and said n+ region are connected together to form a second terminal.

22. The device according to Claim 21 wherein said dielectric layer comprises an oxide.

23. The device according to Claim 21 wherein said semiconductor layer comprises polysilicon.

24. The device according to Claim 21 further comprising:

spacers on the sidewalls of said PIN diode device; and

metal silicide regions overlying said source region, said drain region, said n+ region, and said p+ region.

25. The device according to Claim 24 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.

26. An ESD protection device comprising:

a dielectric layer overlying a semiconductor substrate;

a PIN diode device overlying said dielectric layer wherein said PIN diode device comprises a semiconductor layer having a p+ region and an n+ region that are laterally separated by an intrinsic region; and

a MOSFET device comprising a source region and a drain region in said semiconductor substrate, wherein said PIN diode device is a gate electrode for said MOSFET device, wherein said p+ region forms a first terminal, wherein said drain region and said n+ region are connected together, and wherein said source regions forms a second terminal.

27. The device according to Claim 26 wherein said dielectric layer comprises an oxide.

28. The device according to Claim 26 wherein said semiconductor layer comprises polysilicon.

29. The device according to Claim 26 further comprising:

spacers on the sidewalls of said PIN diode device; and

metal silicide regions overlying said source region, said drain region, said n+ region, and said p+ region.

30. The device according to Claim 26 wherein said first terminal is connected a signal pad and said second terminal is connected to a ground pad.

31. An ESD protection device comprising:

a dielectric layer overlying a semiconductor substrate;

a plurality of PIN diode devices overlying said dielectric layer wherein each said PIN diode device comprises a semiconductor layer having a p+ region and an n+ region that are laterally separated by an intrinsic region and wherein said PIN diode devices are in series; and

a MOSFET device comprising a source region and a drain region in said semiconductor substrate, wherein said PIN diode device is a gate electrode for said MOSFET device, wherein said drain region and said p+ of a first said PIN diode device are connected together to form a first terminal, and wherein said source region and said n+ region of a second said PIN diode device are connected together to form a second terminal.

32. The device according to Claim 31 further comprising:

spacers on the sidewalls of said PIN diode device; and

metal silicide regions overlying said source region, said drain region, said n+ region, and said p+ region.

33. The device according to Claim 31 wherein said first terminal is connected to a signal pad and said second terminal is connected to a ground pad.